CMOS Delay-6 (H.6) Multi-Stage Delay

20161231

Copyright (c) 2015 - 2016 Young W. Lim.

•

Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

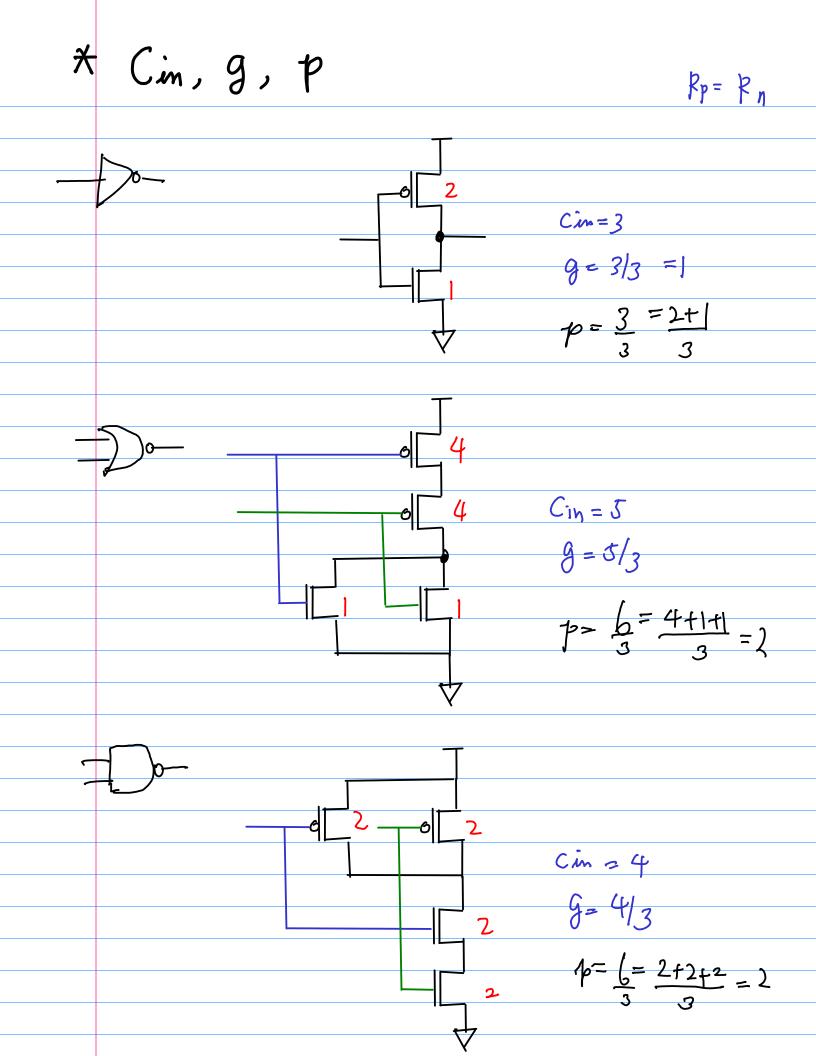
References

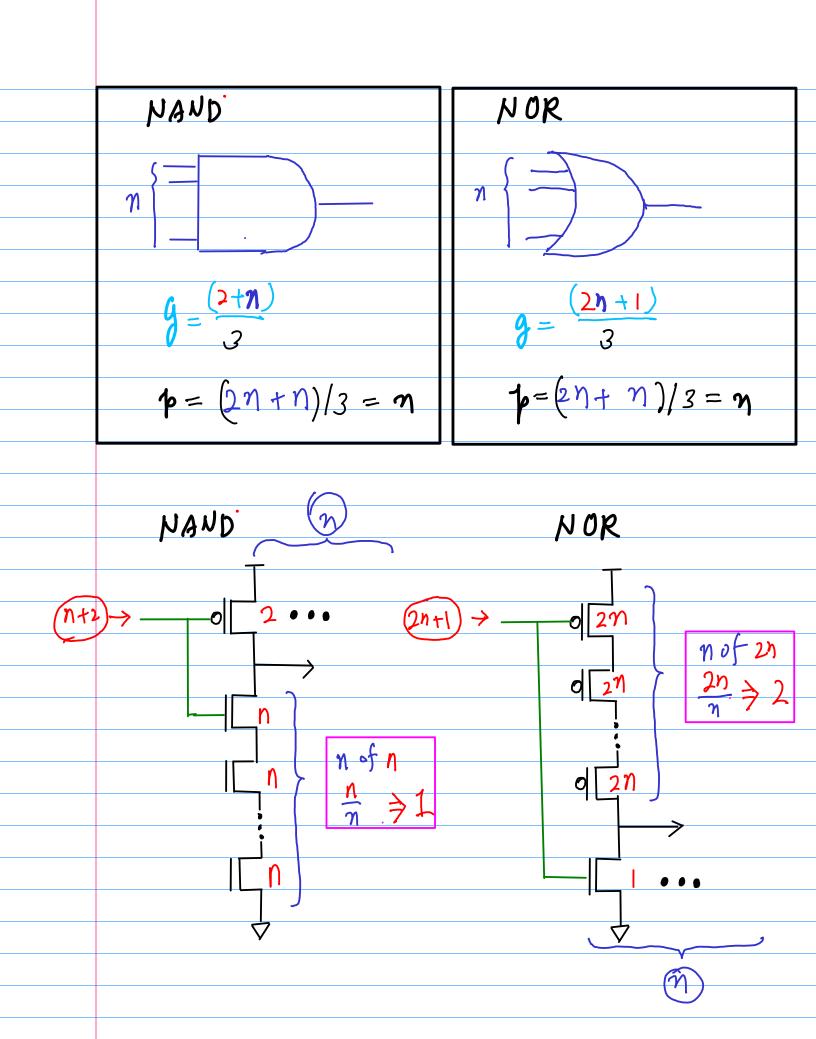
Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
 Weste & Harris Book Site

[2] en.wikipedia.org

[3] http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/notes/Topic%





 $D = N \sqrt[n]{F} + N$ $D = \sum_{i} d_{i} = D_{F} + P$ Path Delay $= \sum_{i} f_i + \sum_{i} p_i$ $\forall i \quad \hat{f} = f_i = g_i h_i = F^{Y_N}$ equal delay $f_1 + f_2 + \dots + f_N = g_1 h_1 + g_2 h_2 + \dots + g_N h_N$ ≥ (g, h,) (g.h) ··· (g. h) F = G HPath Effort F = GBH G = TT gi G = TT gi $H = \frac{C_{out}}{C_{in}}$ $H = \frac{C_{out}}{C_{in}}$ 13 = 1 B = TI bi $D = \sum_{i} d_{i} = \sum_{i} f_{i} + \sum_{i} p_{i}$ = N F ¹/₂ + N

Cout = Cpar t CL Cout = Cpar t CL
$C_{pav} \rightarrow p$ $C_{L} \rightarrow b$
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

In computing **h** (electrical effort) CL Only external cap excluding para cap. Cout = In computing P (parasific capacitance)
 P =
 Cdp + Cdn
 drain parasitis cap

 Cref
 Cin of the ref inventer

 (Symmetric Inventer)

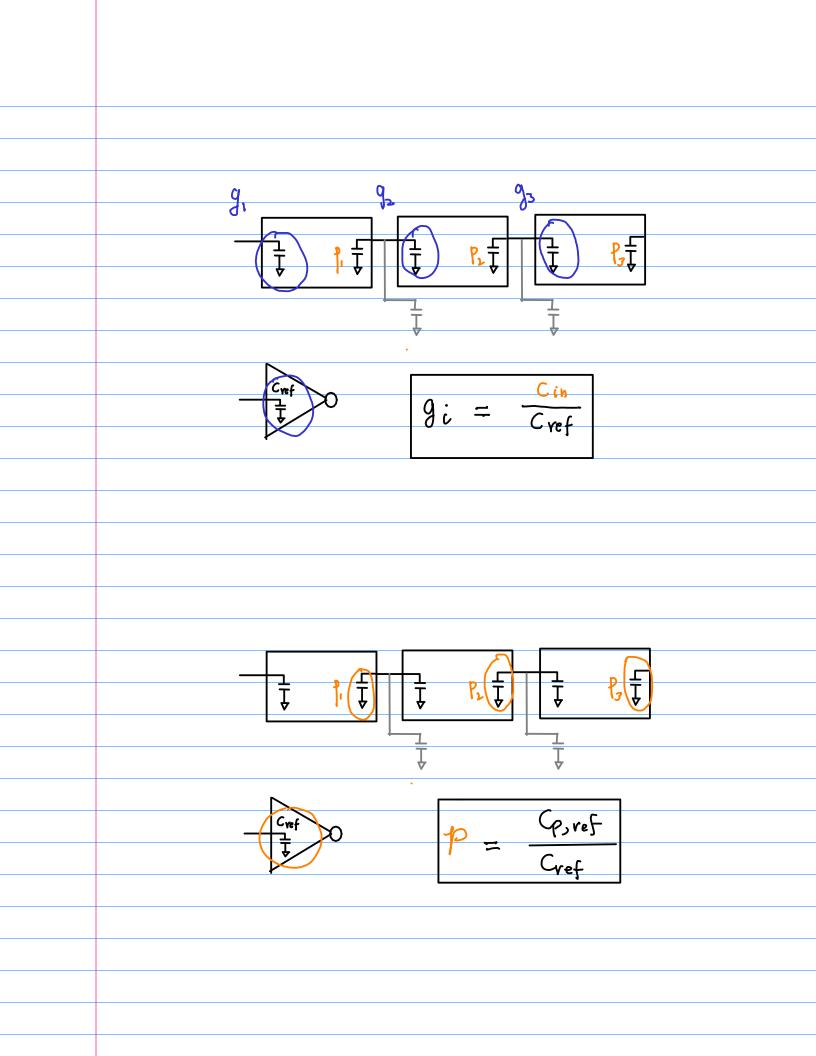
 $g_i = \frac{C_{in}}{C_{vef}}$ Logical Effort $=\frac{C_{out}}{C_{in}}$ Electrical Effort hi $b_{\lambda} = \frac{Conputh + Coffputh}{Conputh}$ Branching Effort Conputh ĥi Cout Cin Cpar 9 -N Pi Cref

 $g_i = \frac{C_{in}}{C_{ref}}$ Logical Effort $h_i = \frac{C_{out}}{C_{in}}$ Electrical Effort Branching Effort bi = Conputh + Coffputh Conputh Cout = hi Cin = bi Conputh = Conputh + Coffpath hi (Cout) < C in ↓ Cpar bi Cpar Conputh Cpar L Cin _ Cin ↓ Cpar

★ Intra Connection → Cin, Cpar logic gate's to pology → Logical Effort f parasitic p -0000 <u>1</u> C in C par <u>-</u> Cont . NAND, NOR, INV, XOR

	X Inter	Connection ectrical fan	design (Cout connection	n →	electric				
		Cin	C	·par.		C in	C pan			
•						C in	C.pu 	r 		
							Civ	1	Cpar]
							4	7	4	

* No Gate Sizing assumed For a given logic gate electrical effort (F) fixed value parasific Slope : logical effort normalized 3 $g = \frac{5}{3}$ delay q î ٩ g= 1 5 parasitic delay g=0 6 independent variable 5 L 2 3 ч Olectrical $f_1 = \frac{Cont}{Cont}$ delay due to only internal cap Without external load cap effort $d = g \cdot h + p$ Æ



Branching Effort	bi = Conputh + Coffputh Conputh
$\frac{C_{in}}{\downarrow}$	$ \begin{array}{c c} C in & Cpar \\ \hline $
7 = R C T must be Conp R Conputh =	Cin Cpar Cin Cpar T T Conputh + Coffputh Conputh + Coffputh) Conputh

× total famout Cap in term of Conputh How many Conputh's in total C in Cpar Conputh Cpar Coffputh Branching Effort bi = Conputh + Coffputh Conputh total famout capacitance normalized by Conputh in terms of Conputh

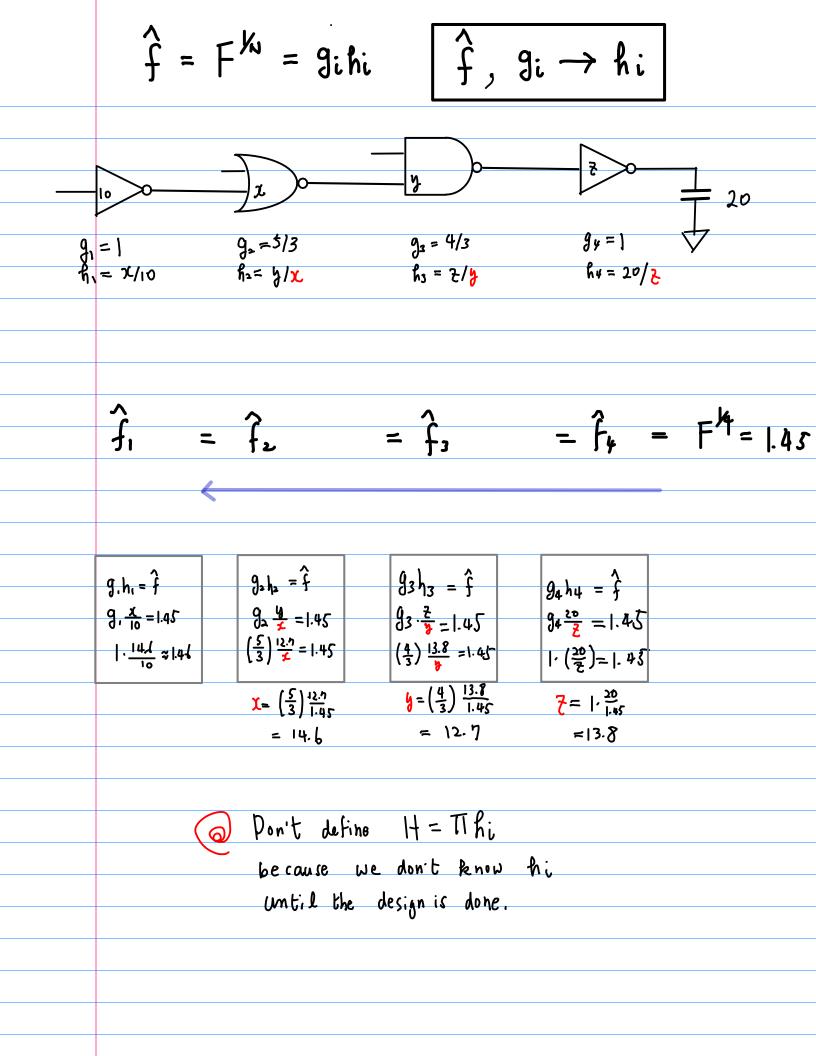
 $g_i = \frac{C_{in}}{C_{vef}}$ Logical Effort $h_i = \frac{C_{out}}{C_{in}}$ Electrical Effort Branching Effort $b_{\lambda} = \frac{Conputh + Coffputh}{Conputh}$ path logical effort $G = \pi g_i$ **path** electrical effort $H = \frac{Cout(path)}{Cin(path)}$ path branching effort 3 = Thi path effort No Branch $F = \Pi f_i = \Pi g_i f_i = GH$ with Branch F = T fi = T bigihi = BGH

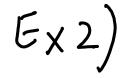
Path Delay D= Zdi = DF + DP = Zfi + Zpi Path Effort below $DF = \sum f_i \gg N \sqrt[n]{TI f_i}$ path Parasitic Deloy $Dp = \sum p_i$ $N\hat{f} = \Sigma\hat{f} = N\sqrt{F}$ $\min D_F \quad f = \Im hi = F^{VN}$ min D = NFW +P Atb 7, Jab > 2ab atb

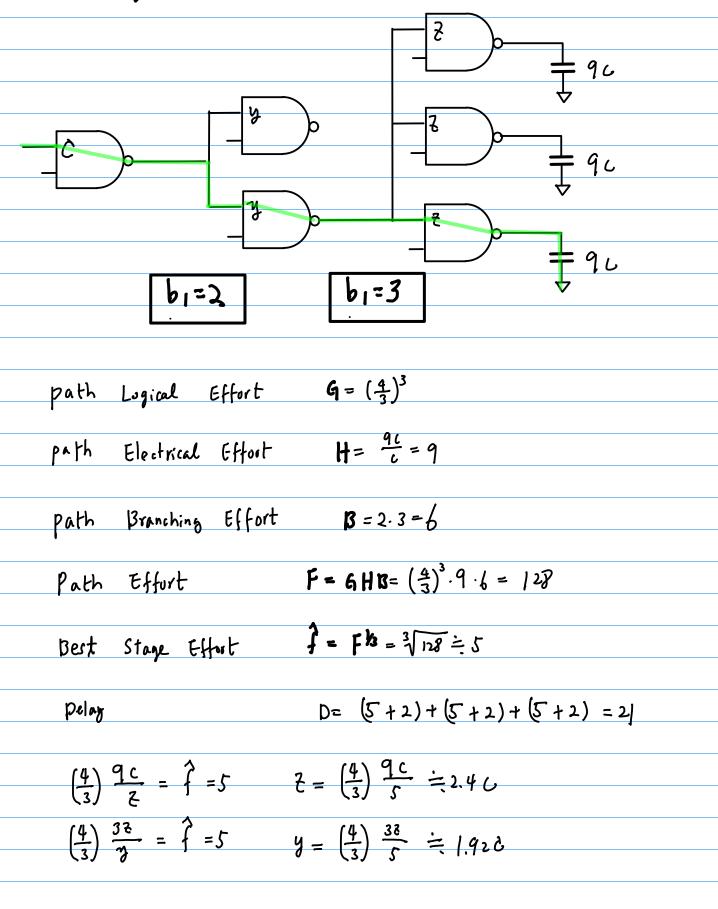
Branching Effort † 90 7 90 $G = g_1 \cdot g_2 = |\cdot| = 1$ $h = h_1 \cdot h_2 = \frac{15}{5} \cdot \frac{90}{15} = \frac{90}{5} = 18$ GH = | x | 8 = 18 $F = f_1 \cdot f_2 = g_1 \cdot h_1 \cdot g_2 \cdot h_2 = \left(1 \cdot \frac{15 + 15}{5} \right) \cdot \left(1 \cdot \frac{90}{15} \right) = 2 \cdot 18$ = 36 F¥GH F=2GH Branching Effort

Ex1) • 2 y 20 0 g₂ = 5/3 h₂= 5/X gz = 4/3 hz = 2/y gy =] $g_1 = 1$ $f_1 = \frac{x}{10}$ $h_{4} = 20/2$ $G = \Pi g_i$ [+= <u>Cout (path)</u> instead of Thi Cin (path) Fi = ∏gihi = GH ← B=1

Ex1) GH y 20 g2 = 5/3 h2= 4/X $g_3 = 4/3$ $g_y = 1$ $g_1 = 1$ $f_1 = x/10$ $h_3 = 2/y$ $h_{4} = 20/2$ path logical effort $G = \Pi g_i = |x + \frac{3}{3} \times \frac{4}{3} \times |z = \frac{20}{9}$ path electrical effort $H = \frac{Cout(path)}{Cin(path)} = \frac{20}{10}$ $\frac{(2\cdot n+1)}{3} = \frac{5}{3}$ $\frac{(2+n)}{3} = \frac{4}{2}$)0— $F = G \cdot H = \frac{20}{9} \times \frac{20}{10} = \frac{20^2}{90}$ $f = F / q = \left(\frac{400}{00} \right) / q = 1.452$

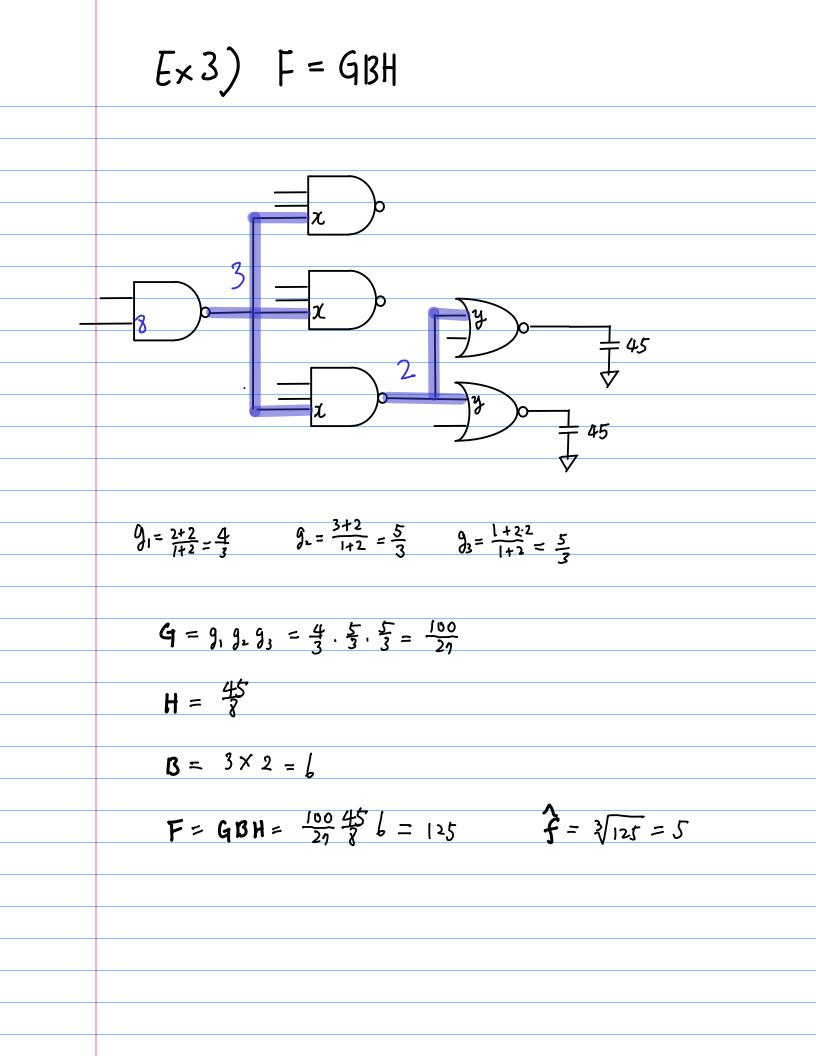


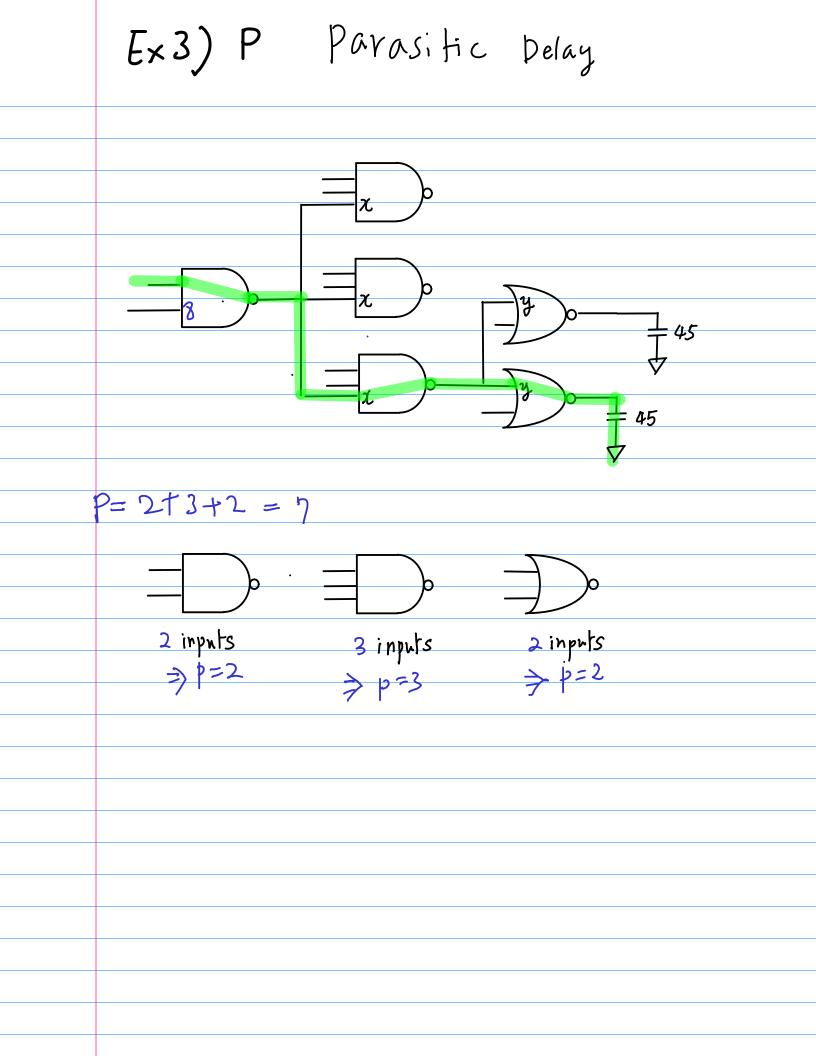


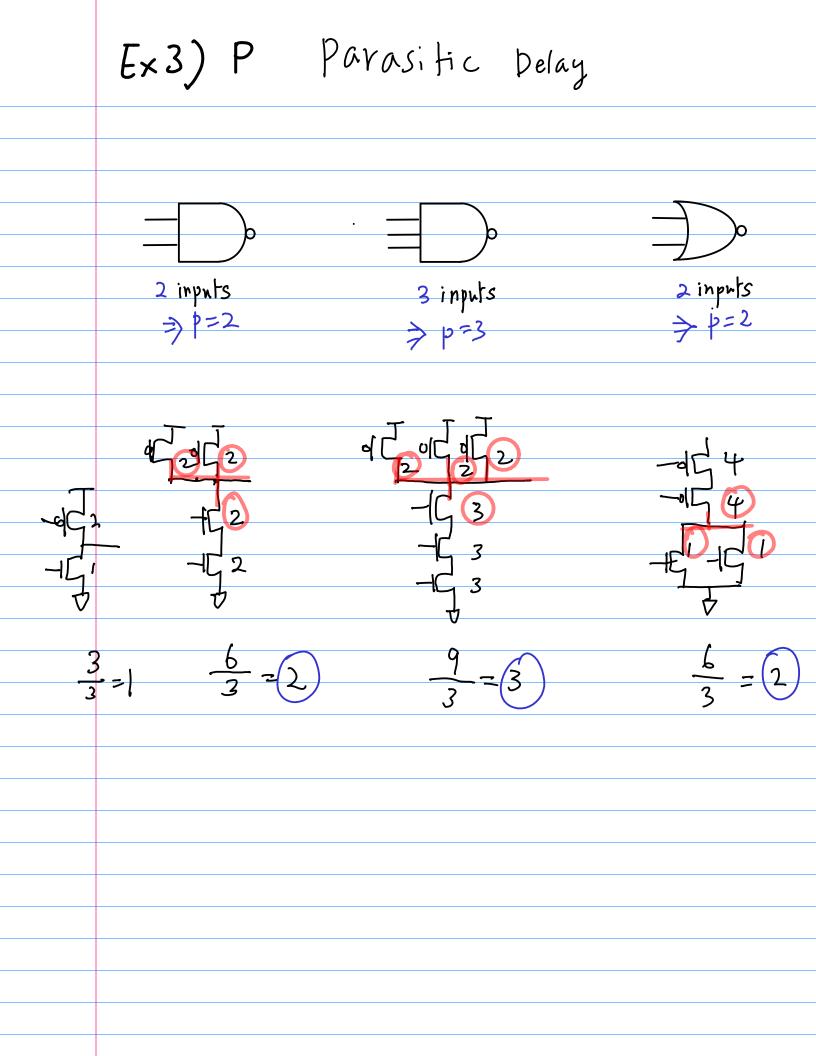


Ex2) BGH 2 :90 y 2 ± 90 Y = 96 $G = (\frac{4}{3})(\frac{4}{3})(\frac{4}{3}) = (\frac{4}{3})^3 = -0 - \frac{(2+n)}{3} = \frac{4}{3}$ $= \frac{qc}{c} = q$ H qc $B = \begin{pmatrix} \frac{2^{1}}{3} \\ \frac{3^{2}}{3} \end{pmatrix} \begin{pmatrix} \frac{3^{2}}{2} \end{pmatrix} = 2 \cdot 3 = 6$ C $F = BGH = 6 \cdot \left(\frac{4}{3}\right)^3 \cdot 9 = 2 \cdot 7 \cdot \frac{4^3}{2^3} \cdot 9 = 128$

Ex2) y, z 2 ± 90 y b ± 9c Y = 9. 32 91 = 4 93= 43 g_ = 4 h2= 32 $h_3 = \frac{q_c}{z}$ $h_1 = \frac{2y}{c}$ $\hat{f} = g_1 \hat{h}_1 = |\hat{f} = g_2 \hat{h}_2| = |\hat{f} = g_3 \hat{h}_3| = \sqrt[3]{128} = 5.0$ $\int = \begin{pmatrix} 4 \\ 3 \end{pmatrix} \frac{24}{C}$ $\int = \begin{pmatrix} 4 \\ 3 \end{pmatrix} \frac{32}{V}$ $\int = \begin{pmatrix} 4 \\ 3 \end{pmatrix} \frac{9C}{2}$ $= (\frac{4}{3})^{\frac{1}{2}} \frac{1}{2} \frac{1}{2$ = 5.12 2 = 2.40 y = 1.92C

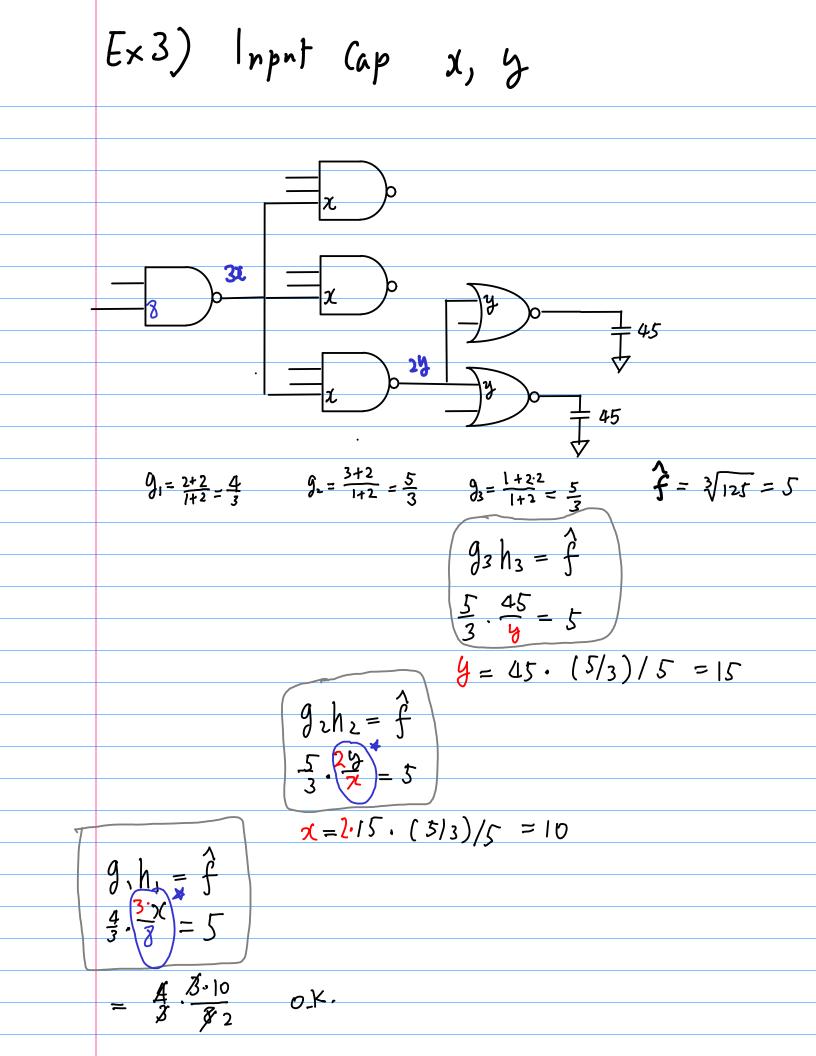


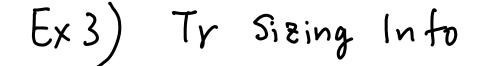


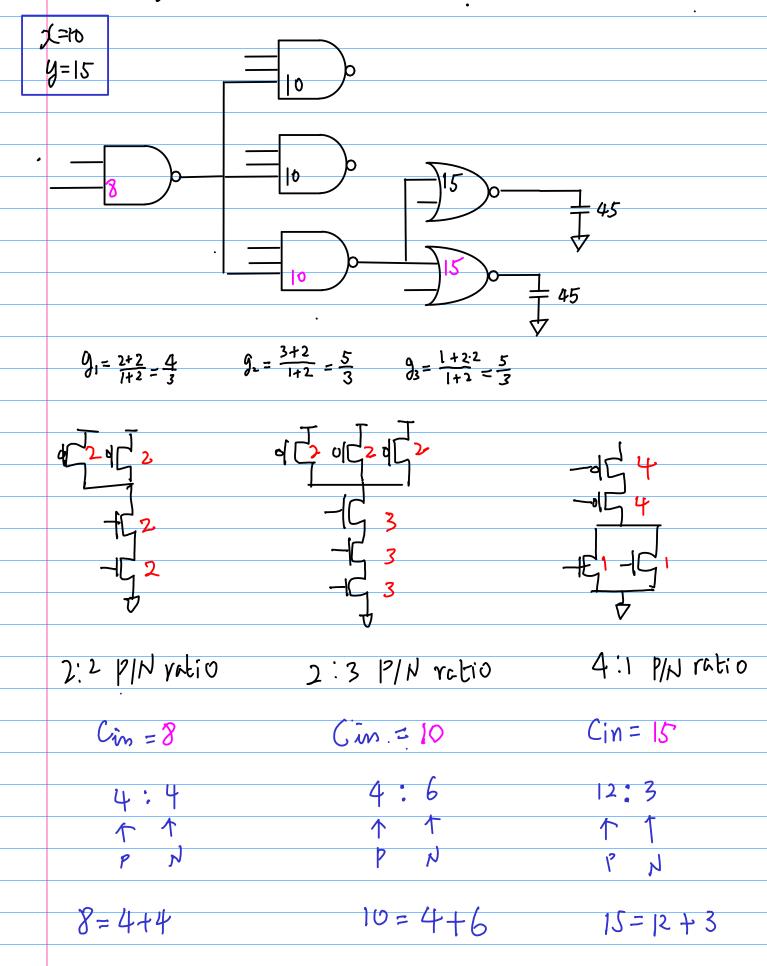


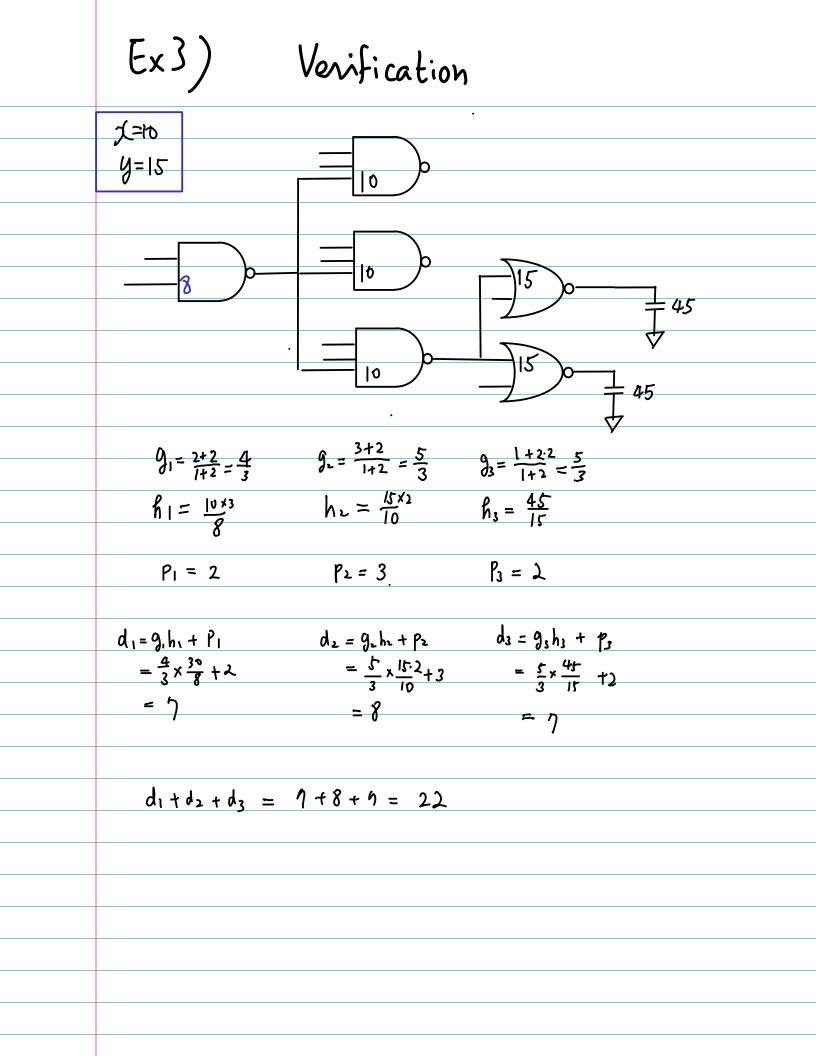
Ex3) Min Path Pelay $\min \text{ path delay } D = NF^{W} + P$ $= 3\sqrt[3]{125} + 7 = 3.5 + 7 = 22$ 22 / 5 = 4.4 × FO4 delay F04: d= h+1 = () F04 (Invater with fanout = 4) g.h+p= h+1=5

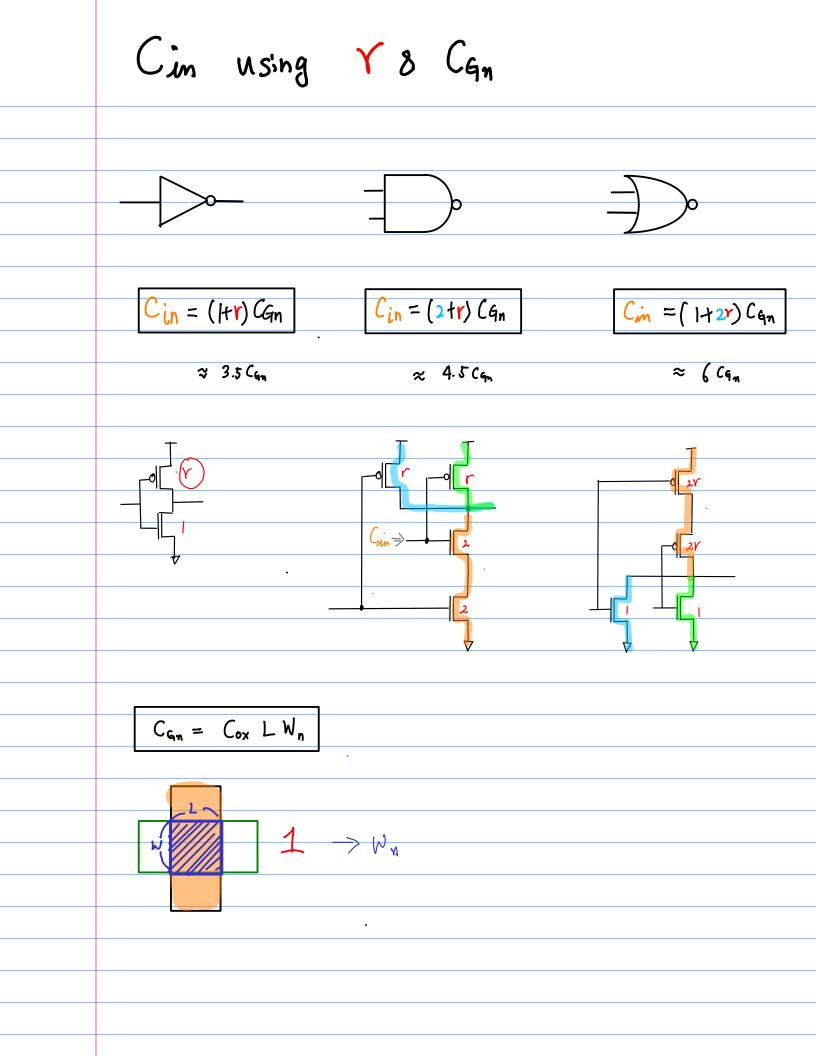
Ex3) FO4 Invator Delay Fanout-of-4 g = | h = 4 |)= Pinv = 1 d = gh + p = 5Useful metric to Characterize process 57

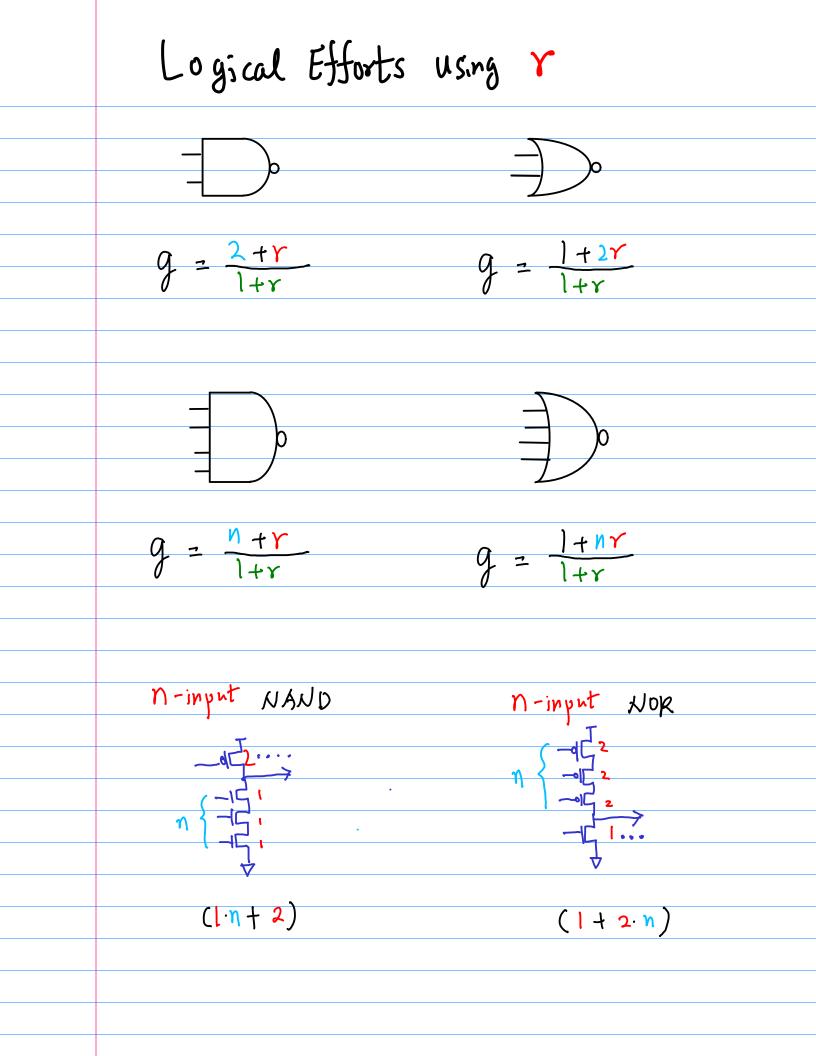


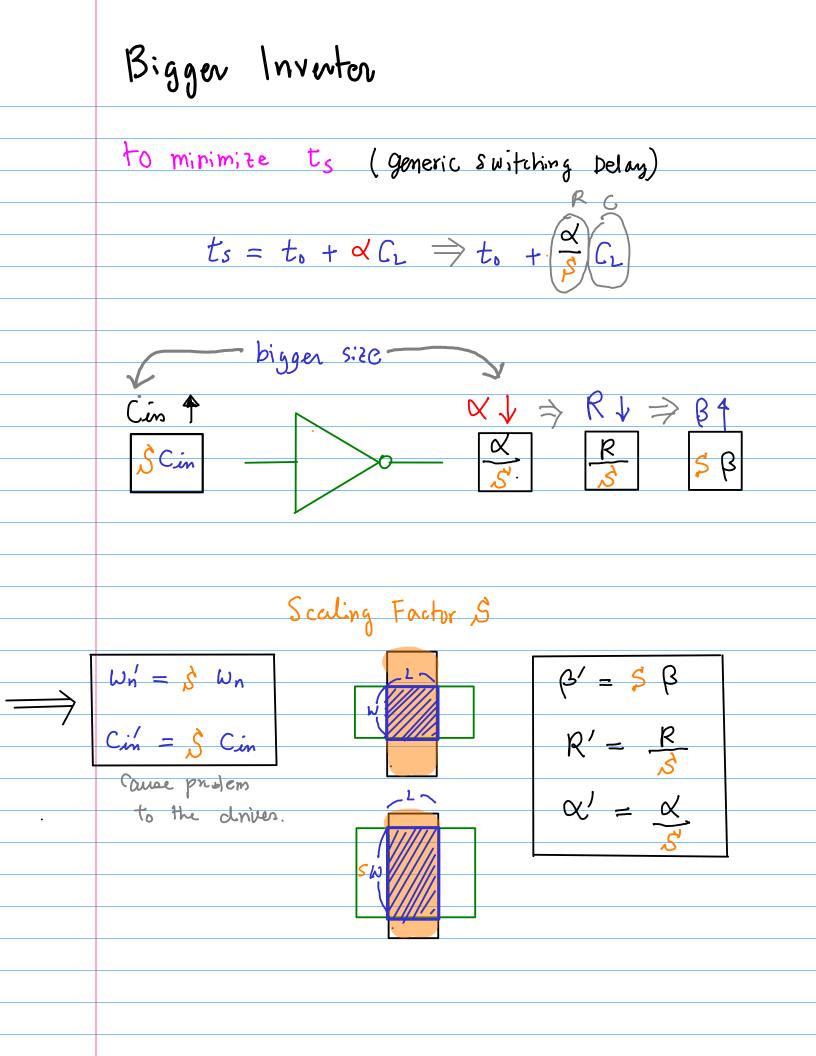




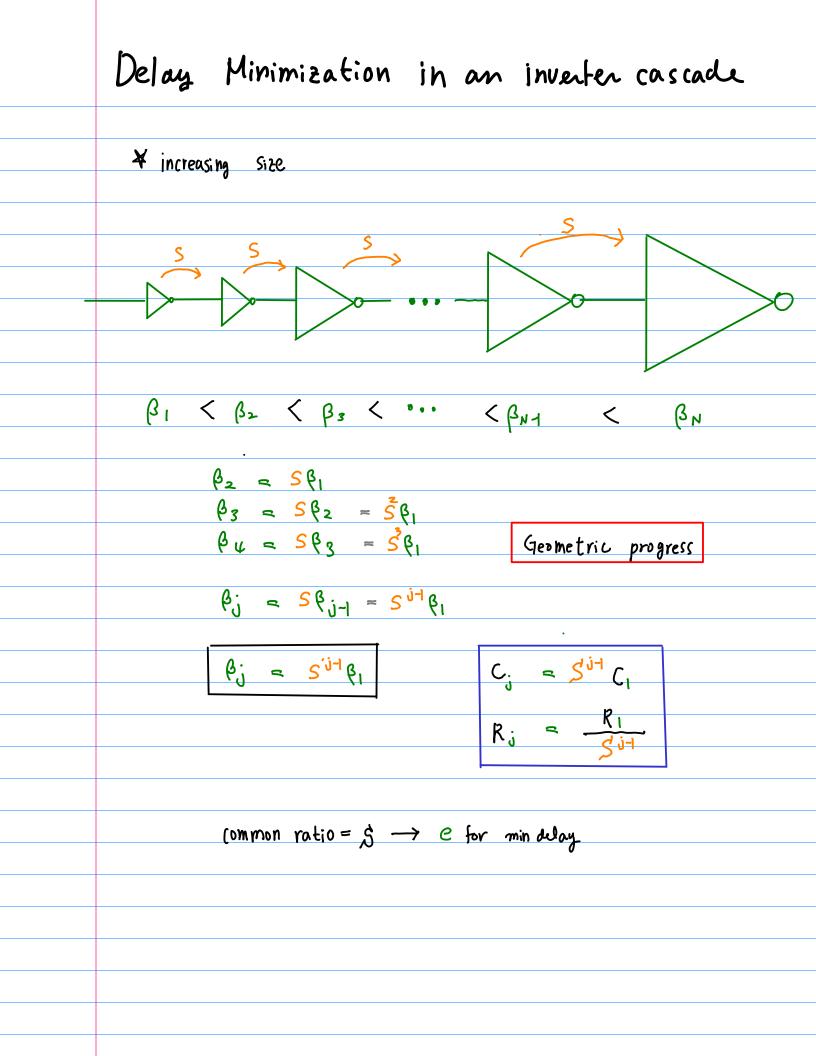








think G.P. (Geometric Progression) in Sizc factors S ⊬ Arithmetic Progression >/ Geometric Progression min delay Z path delay when all equal path delay



Ex4) F=GH- C 3 C 4 $G = (1)(\frac{1+2r}{1+r})(\frac{2r}{1+r}) = 2.2$ (r=2.5) $|1 = \frac{C_{\chi}}{C_{1}} = \frac{500}{20} = 25$ $F = G H = 2.2 \times 25 = 55$ the optimum stage effort $\hat{f} = F^{V} = (55)^{V_3} = 3.8$ parasitic dulay term P= P1 + P2 + P3 the total path delay $\hat{B} = NF^{W} + P = 3(3.8) + P = 11.41 + P$

Ex4) Input Capacitonce C₁, C₂, C₃

$$f_{2} h_{3} = \frac{2}{1-3}g \qquad (h) = (h^{2}h)/(h^{2}h) = 45/35 = 1.29 \quad (hAND)$$

$$f_{3} = \frac{2}{1/9} = \frac{3.8}{1.24} \quad (h) = 2.97 = C_{4}/G$$

$$f_{3} = h_{3} = \frac{2}{1/9} = \frac{2}{1.24} \quad (h) = 2.97 = C_{4}/G$$

$$f_{3} = \frac{2}{1/9} = \frac{2}{1.24} \quad (h) = \frac{2}{1.24} = \frac{2}{1.24}$$

Ex4) Scaling Factors 51', 52, 53 $S_1 = \frac{C_1}{3.F(GN)} = \frac{20}{3.F(GN)} = \frac{5.91}{(Gm)}$ $S_2 = \frac{C_2}{6 G_n} = \frac{1635}{6 C_{q_n}} = \frac{12.125}{C_{q_n}}$ $S_3 = \frac{C_3}{4.5 C_{6n}} = \frac{169.5}{4.5 C_{6n}} = \frac{37.69}{C_{6n}}$ $S'_{1} = \frac{S.91}{C_{m}} / \frac{S.91}{C_{m}} = 1$ $S_{2} = \frac{12.\eta_{25}}{G_{m}} / \frac{5.\eta_{1}}{G_{m}} = 2.23$ $S_3 = \frac{37.67}{C_{sm}} / \frac{5.91}{C_{sm}} = 6.60$

N inverters (odd number) g = <u>Cin</u> = <u>Cvef</u> = | h = Cout = Cref = | $P = \left(\frac{C_{p, ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right) = \frac{3}{3} = 1$ d = gh + p = 2dals = 27 $freg = \frac{1}{2N dats} = \frac{1}{4NC}$